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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,212	05/31/2001	Omar Kebichi	1011-58140	1993

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	7

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,212	KEBICHI ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Pursuant to 35 USC 131, **Claims 1-36** are presented for examination. The Examiner has considered the Applicant's IDS of 8 Jan. 2002. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Art Unit 2133.

Claim Rejections - 35 USC ' 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language..

1.1 Claims 1-3, 8, 12 are rejected under 35 U.S.C. 102 (e) as being unpatentable over **Applicants' admitted prior art.**

As per Claims 1-3, 8, 12, Applicants admit as prior art the claimed IC with BIST arrangement comprising plural BIST controllers, resume input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM in **prior art** Fig. 1 and related description.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. 0 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2.1 Claims 4-7, 9-11, 13-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Phan** (US Patent No. 6651202).

As per Claims 4-7, 9-11, 13-36, Admitted prior art substantially discloses the claimed IC with BIST arrangement comprising plural BIST controllers, resume input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM, IDDQ/walking/testing means in **prior art** Fig. 1 and related description.

Not specifically described in detail in Admitted prior art is the step of state machine controlling means for synchronization. **However,** such state machine controlling means is well known. **For example, Phan,** in an analogous art, discloses a **BIST arrangement** in Fig. 1: BLOCK 102 and related description.

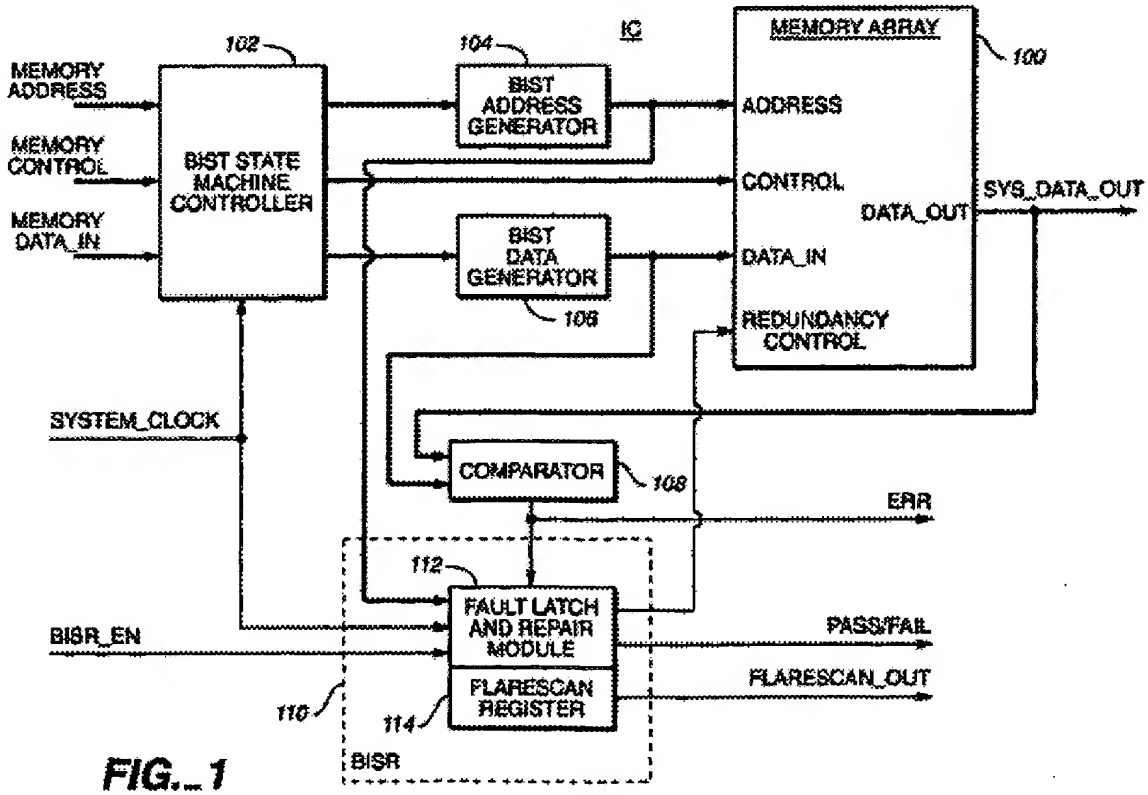

FIG._1

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Admitted prior art** by including therein state machine controlling means OPERATION TIMING for each of **plural BIST controllers**, as taught by **Phan,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique whereby "*The outputs of the BIST address generator 104 thereby control the address inputs of the memory array 100 during execution of a test pattern algorithm. Thus, the BIST address generator 104 and BIST data generator 106 may provide address and data sequences, respectively, to the memory array 100 in an order as specified by a test pattern algorithm. Preferably, such sequences provide a set of data bits in a pattern that maximizes fault coverage for detecting various types of faults within the memory array 100. A system clock signal SYSTEM_CLOCK is also provided to both the BIST state machine controller 102 and the BISR circuitry 110 for logic clocking and synchronization.*" {See **Phan,** col. 4 line 29 et seq.}

2.2 Claims 4-7, 9-11, 13-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Huang et al.** (US Patent No. 6415403; Jan. 29, 1999).

As per Claims 4-7, 9-11, 13-36, Admitted prior art substantially discloses the claimed IC with BIST arrangement and HDL means therefor comprising plural BIST controllers, resume input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM, IDDQ/walking/testing means in **prior art** Fig. 1 and related description.

Not specifically described in detail in Admitted prior art is the step of state machine controlling means for synchronization.

However, such state machine controlling means is well known. **For example, Huang et al.,** in an analogous art, discloses a **BIST arrangement** In FIGs. 3-4 and related description.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Admitted prior art** by including therein state machine controlling means OPERATION TIMING for each of **plural BIST controllers**, as taught by **Huang et al.**, because such modification would provide the procedure disclosed in **Admitted prior art** with a technique whereby "When the BAC control signal is high, a logical one, the BIST circuit is activated to test the embedded memory 13. All signals are synchronized with the BIST clock, BCK. The BRS signal is pulled high along with BCS at the beginning of the BAC control signal to perform a scan test to verify that the BIST controller is operating correctly. Scan chains are formed between BSI and BSO to apply patterns and collect responses. When the scan test is completed the BRS signal is pulled low to reset the BIST controller, and BCS remains low to generate a reset sequence. The BRD and BGO signal are also brought low, and the BIST controller performs a scan test for the remainder of the BIST circuitry. Once the scan test is completed, a test algorithm is applied to the embedded DRAM 13 in accordance with the control sequence of the finite state machine shown in FIG. 2. At the end of the test sequence BRD is brought high and BGO is sampled to read out the test results. Then BAC is set to a low state to return the DRAM 13 to normal operations. " {See **Huang et al.**, FIG. 3 and related description.}

Claim Objections

4. Claims 35-36 should depend on Claim 34; Claim 4 line 2 should read 'and [the] further.' Appropriate correction is required.

Conclusion

4.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, **Fourth Floor** (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.
Patent Examiner
2/28/04